



Serial No.: 10/605,110

Art Unit: 2825

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Anthony I-Chih Chou	Date:	11 August 2004
Serial No.:	10/605,110	Art Unit:	2825
Filing Date:	09 September 2003	Examiner:	Belur V. Keshavan
Confirmation No.	2109	Docket No.	FIS920030288US1
Title:	Method for Separately Optimizing Thin Gate Dielectric of PMOS and NMOS Transistors within the Same Semiconductor Chip and Device Manufactured Thereby	Attorney:	Graham S. Jones, II 42 Barnard Avenue Poughkeepsie, NY 12603-5023

AMENDMENT

The Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Your Honor:

In response to the Office Action of 13 May 2004, please amend the above-identified application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.